ALLEN W. BLACK

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Skill Summary:

- **Embedded Systems:** system design, firmware design, digital hardware design, system integration and test
- **Realtime Systems:** many hard and soft realtime projects; VxWorks, TI SYS/BIOS / DSP/BIOS, CMX-RTX, SPOX, Embedded Linux, Embedded DOS, pthreads, and a variety of homebrew / bare-metal realtime "operating systems" / super loops
- **C/C++/Java Programming:** C / C99; C++; Java; GNU, Eclipse, Wind River Workbench, Microsoft Visual Studio, IAR Embedded Workbench, TI Code Composer Studio, Freescale CodeWarrior, and Microchip MPLAB development tools; embedded, DOS, Windows, Linux, and other UNIX applications; Android mobile development
- **Microprocessor Architectures and Assembly Language Programming:** ARM V7 / Cortex-A15, Cortex-A8, Cortex-M4, ARM9TDMI cores, TI DaVinci media processors DM8148 & DM365, Microchip PIC24, TI MSP430, Freescale ColdFire, TI C674x, C67xx, and C64xx DSPs, Renesas SH-2 and M16C, 80x86, 680xx, 8051, Analog Devices SHARC, 210xx, and 210x DSPs; bare-metal boot loaders, development/debugging monitors, interrupt processing, cache coherency, MMU programming, device drivers, and algorithm optimization
- **Device Driver Programming:** touchscreen input, bitmapped display output, SPI, I2C, I2S, CAN, asynchronous serial / RS-232 / RS-485, PCI Audio cards, integrated audio chips, AES-EBU, Flash memory, Ethernet switches, PLL frequency synthesizers, DDS chips, GPIO, MIL-STD-1553, many other miscellaneous devices
- **Linux Programming:** GNU, gcc, g++, gdb, make, Autotools, kbuild, Git, CVS, SVN (Subversion), U-Boot, GTK+, Qt; soft realtime embedded Linux, kernel space device drivers, user space device drivers, desktop applications
- **FPGA/CPLD Design:** Verilog, VHDL, AHDL, ABEL, and schematic capture design input; Altera Quartus, SOPC, MaxPlus2, and Xilinx ISE integrated environments; Altera Stratix, Flex 8K, Acex 1K, Max 7000 and Xilinx Virtex-E, and XC4000 architectures; NIOS CPU core and many other IP blocks from Altera and Xilinx, Modelsim and Aldec simulation
- **Hardware Design:** schematic capture design input; OrCAD Capture, other Cadence and Mentor Graphics tools; digital design, mixed signal design, PCI bus interface, JTAG interface; board layout and routing supervision; system integration and test
- **RF and Microwave Communications Systems:** HD digital broadcast radio, spread spectrum systems, fixed tuned systems, frequency synthesis - National Semiconductor, Motorola/Freescale, and Fujitsu synthesizer control and direct implementation in FPGAs, data protocols, error detection and correction techniques, Viterbi FEC
- **User Interface Programming:** windows, menus, keyboard, mouse, event-driven programming; all types of front panel input devices from touchscreens with smart buttons and menus to software debounced push buttons and jog wheels with quadrature optical inputs; all types of displays from discrete LEDs to flat panels with bitmapped graphics and fonts
- **Digital Signal Processing:** RF up-conversion, clock discipline and synchronization, digital audio, image, and video processing, radar signal processing algorithms, multiprocessing systems, intrinsics / assembly language optimizations

Education:

1985 Graduated with B.S. in Electrical Engineering from The Pennsylvania State University (emphasis on Microprocessor Systems and Assembly Language Programming).

1989 Completed graduate courses (Microprocessor System Design, Digital Signal Processing) from Fitchburg State University.

2007 Completed Linux Server Configuration and Administration course from Spidertools.com.

Ongoing Near constant self-education in my core competencies as well as other technical subjects of interest (i.e. - Android development, Python, GPU / parallel programming, etc.). Typically read 20+ technical books a year and have enjoyed subscriptions to Circuit Cellar, Nuts & Volts, EE Times, Embedded Systems Programming, Linux Journal magazines and many others for over 20 years. Attend the Embedded Systems Conference in Boston and learn from vendor sponsored seminars as often as possible. Attended 2016 Black Hat Conference / Briefings. Audit online university courses (e.g. Network Design and Security, Algorithms) via Coursera.com from time to time. Recent employer sponsored training in Cryptography Engineering, Cyber Security, Digital RTL Hardware Design, and High-speed PCB Design.

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Experience:

2013 – Present Employed by Northrop Grumman of Linthicum, Maryland. Embedded Software Engineer within the Mission Security section of the Mission Systems division. Designed, coded, and integrated Assembly, C, and C++ embedded systems firmware. Low-level ARM system programming within a ARM V7 SMP architecture. Low-level and application level programming within a Renesas Super H2 architecture. VxWorks RTOS kernel driver and real time process programming. Debug and integration of VHDL/RTL ARM V7 SoC hardware. Extensive experience with ARM DS-5 debugger, Synopsys QuestaSim, Wind River Workbench, Jenkins continuous integration, SmartBear Collaborator code review, and Git source code management tools. Agile process and ScrumMaster training and experience. Northrop Grumman Cyber Academy training and attended the 2016 Black Hat Conference / Briefings. DOD Top Secret (SSBI) and SAP clearances obtained and are current.

2011 – 2013 Consulted for AWB Technologies of Wrightsville, Pennsylvania. Projects as follows:

- Android Application Development: Designed and coded the SpaceStuff game available in the Google Play app store. This Android application was written in JAVA using the standard Android APIs. It encompassed a multiple screen graphical user interface, accelerometer sensor input and processing, 2D realtime graphics processing and rendering, and network communications. To host a "World Leaderboard" for the game, a website and webserver application were also developed using HTML5, CSS, and PHP accessing a MySQL database for storage of user registration, score information, and other gameplay analytics.

- Video Analytics IP Camera: Designed and coded C and C++ firmware to support custom video analytics algorithms running on a TI DaVinci DM8148 media processor within a 10 MegaPixel IP camera reference design. The DM8148 processor contains 4 heterogeneous cores (one ARM Cortex-A8, two ARM Cortex-M4s, and one TI C674x DSP) and runs 2 different operating systems (Embedded Linux and TI SYS/BIOS). Development was performed within TI's Multi Channel Framework (MCFW) and used many other TI and open source APIs. Many modifications and additions needed to be made to this framework and to other TI supplied firmware for this extremely complicated heterogeneous multi-processor system. Ultimately, firmware was developed that ran on all 3 types of cores and under both operating systems. All code was configured under the Git distributed revision control system. And a number of Bash scripts were developed to support installation and building of firmware releases.

- DOD ANS Program: Designed and coded firmware (C and Assembly code built and debugged with the Microchip MPLAB IDE) to perform system monitoring and error reporting for the ACS (Advanced Computing Subsystem) subsystem of the DOD ANS (Autonomous Navigation System) program. The ACS subsystem was comprised of a hardened VME backplane with multiple circuit cards including multiprocessor CPU and GPGPU computational units, high-speed fiber I/O, storage, and power supply monitoring and control units. The system monitoring and error reporting firmware ran on Microchip PIC24 microcontrollers. It utilized an I2C bus in a multi-master configuration for communication between the various cards. Message definitions and messaging protocols were developed for all communications between the cards.

- Embedded Linux Kernel Module for USB Video Camera: Assisted in the backporting of a USB WebCam Gadget kernel module to work with a MontaVista realtime kernel used with TI's DVSDK (Digital Video Software Development Kit). This work supported the Leopardboard TI DaVinci DM365-based video camera platform.

2009 – 2010 Consulted for Zeus Technology Systems of Linthicum, Maryland. Project as follows:

- Miniature Microwave Tuner: Designed and coded all firmware (C and Assembly code built and debugged with the IAR Embedded Workbench IDE) for five unique boards comprising a miniature microwave tuner. The extremely low noise tuner (a 2nd generation redesign of the ZSR-010 product) features frequency coverage from 20 MHz to 10 GHz tunable to 1 Hz resolution. One board, containing an ARM9TDMI / ARM920T core microcontroller (Atmel AT91RM9200), provided the USB and RS-232 user interfaces and acted as the master controller for the other four boards commanding them via direct serial data links. The four satellite boards each contained an MSP430 microcontroller (TI MSP430F2617), off-chip serial flash memory for storing factory calibration data, and a variety of digitally controlled RF circuitry (i.e. - PLL frequency synthesizers, direct digital synthesizers, DAC voltage controlled attenuators, RF signal path analog switches, etc.) Since each satellite board contained a different portion of the RF circuitry, five unique firmware images needed to be generated and coordinated for the system. In addition to manual tuning under user control, the system provided fast sweep/scan tuning driven by user entered frequency tables stored in nonvolatile FeRAM on the main controller board. An AGC control loop was also implemented in firmware running on two of the satellite boards communicating directly with each other autonomous from the the main controller board.

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2009 Consulted for Harris Broadcast Systems Division of Mason, Ohio. Project as follows:

- Main Controller Module with Touchscreen: Assisted a team doing firmware programming for the Main Controller Module used to control a number of Harris' recently introduced TV and radio transmitter products. The module is rack mounted at a broadcast facility and provides a backlit LCD touchscreen as the primary local user interface. The module contains a ColdFire MCF5484 microcontroller and a variety of interfaces (3 CAN bus transceivers, RS-485, RS-232, GPIO, USB, etc.) used for control and status to/from other broadcast devices both local to the equipment rack and to/from remote devices. A Marvell Link Street (88E6060) 6-port Ethernet Switch was also included on the module to allow the user interface to be viewed and controlled remotely from a web browser and also to provide a LAN connecting other equipment in the broadcast facility. The firmware for this project ran in a soft realtime embedded Linux environment (kernel version 2.6.28 compiled for the ColdFire V4 core architecture with several custom and several modified device drivers) and for the most part was managed and compiled using the open source LTIB (Linux Target Image Builder) tool and loaded using U-Boot. A wide variety of duties were performed on this project. Debugged and patched a non-working (for this platform) CAN kernel driver. Similarly debugged and patched the Linux touchscreen library, tslib, and the kernel driver for the Burr-Brown ADS7846 touchscreen controller. Wrote a driver for initializing the Marvell Ethernet Switch. Assisted in porting display graphics from the Nano-X library to the DirectFB library (done for performance reasons). Then evaluated solutions for running an embedded web browser (required for remote control and status of other broadcast system units) on the module. After this evaluation, successfully ported the commercial Unicoi Systems WebPilot web browser to run under DirectFB.

2002 – 2008 Consulted for iBiquity Digital of Columbia, Maryland. Projects as follow:

- Embedded Exporter: Worked on a project to re-architect the reference HD Radio exciter design. Selected development board (Innovative DSP's SBC6713e) for the re-partitioned part of the design known as the Embedded Exporter. Developed basic skeleton code and communication drivers for both the DSP (TMS320C6713 running under DSP/BIOS realtime operating system) and host (embedded Linux running on an Intel Pentium processor) sides of the re-partitioned design. The DSP-side communications driver utilizes burst-mode DMA transfers through a FIFO to an on-board TCP/IP coprocessor. The host-side driver utilizes standard Linux Ethernet function calls.

- Exciter-On-A-Stick: Designed prototype hardware for a handheld device which under user control plays back several minutes of a “canned” HD Radio RF waveform at a low power level. This prototype was handed off to a commercial design and manufacturing partner who is now producing it for HD Radio testing, demonstration, and promotion. Developed a complex state machine, implemented within an Altera Max7000 CPLD, to handle the user interface and waveform retrieval from flash memory and subsequent synchronized playback through up-converting RF circuit elements. The CPLD also handled tuning of an RF carrier synthesizer chip. Assisted with prototype component selection, schematic capture, and circuit board layout.

- Digital Up-Converter: Designed the 3rd generation digital up-converter module used in current generation HD Radio exciters. Significantly reduced parts count and board complexity (over the 2nd generation module) by using an Altera Stratix FPGA to handle all PCI interface, DSPdigital up-conversion, FIFO and buffer RAM functionality. Also greatly increased module flexibility and testability by incorporating a NIOS CPU core with an Avalon switch fabric parameterized bus in the same FPGA. This project was a large and varied undertaking with responsibilities including: schematic capture with handoff to board layout and manufacturing vendor with much attention given to the mixed signal nature of the module and its grounding and layout requirements, a complex FPGA design written in VHDL covering elements previously mentioned, a reverse engineered implementation of DSP functionality contained in a TI Graychip GC4116 digital up-converter IC, various improvements to analog conversion and driver circuitry, Linux device driver design, NIOS CPU core driver programming, as well as prototype board debug, integration and test.

- Remote Clock Synchronization for Exgine Exciter: Implemented DSP processing in an Altera Stratix FPGA to synchronize two 10 MHz oscillators physically separated by tens of miles connected only via an STL microwave link. This complex problem was solved by detecting constant but jittery messages transmitted across the STL link at a rate of approximately 0.6 Hz. These events were passed through an IIR filter network to generate a phase error signal which drove a DAC to gradually pull the remote VCXO into phase and frequency alignment. The IIR filter network required a very slow response time (approximately a 10 hour time constant) as over-the-air broadcast signals were derived from the remote oscillator and stringent FCC requirements needed to be met.

- Exgine Exciter Device Drivers and Hardware Interface: Designed hardware interface and device drivers for 3rd generation HD Radio exciter reference design known as Exgine. This 3rd generation design physically separated transport modem

computation from audio and data processing. The modem functionality was moved to a TI TMS320C6415 DSP running the TI DSP/BIOS realtime OS. Device drivers and peripheral support functions were written for the TMS320C6415 platform to allow communication with a new Linux device driver (also designed and written) via a PCI bus. Provisions were made to allow future implementations of the exciter front end processing to be moved to other platforms with communications occurring via a hardware fifo and hardware interrupts. The entire system was successfully implemented using a modified COTS Valley Technologies VT-1420 PCI card.

- Linux Device Drivers and SMP Kernel Level Debugging: Wrote and maintained a Linux device driver for the custom station interface module used in the HD Radio reference exciter system. Debugged, maintained, and improved several other Linux device drivers used in the HD Radio reference exciter and reference receiver systems including drivers for a custom digital up-converter module, a custom digital down-converter module, and for several SEKD ProDif96 digital audio cards. Also assisted in analysis and debugging of various Linux kernel level issues affecting the HD Radio reference exciter running on an SMP Pentium platform.

2001 – 2002 Consulted for Zeus Technology Systems of Linthicum, Maryland. Projects as follow:

- 2.4 GHz Spread Spectrum Transceiver: Designed and coded all firmware (C and Assembly code for Renesas M16C62 microprocessor) for a frequency hopping transceiver. Data was input and output via asynchronous serial ports using a proprietary datagram protocol. Supported connectivity options included point-to-point, host-to-multipoint, and repeater modes. Firmware performed realtime control of a National Semiconductor LMX2350 Dual Frequency Synthesizer as well as many other discrete RF functions. Also implemented Blowfish encryption algorithm (on the embedded system and on a PC) to protect intellectual property during user installable firmware upgrades to flash memory.

- Miniature Panic Button Transmitter and Receiver: For the transmitter, designed Altera FPGA (Max 7000) which contained a Frequency Synthesizer unit and a Data Sequence Generator. For the receiver, designed a Xilinx FPGA (Virtex-E) which contained interface logic to a microprocessor bus, tuning control for a Motorola (now Freescale) Frequency Synthesizer, and a 4096 tap correlator to detect the panic data sequence in high noise environments.

- VME Radio: Designed Altera FPGA (Acex 1K) which translated between a Cypress SVIC chipset connected to a VME bus and a microprocessor bus (Renesas M16C62). The FPGA performed power-on initialization of the SVIC chips as well as providing a dual-ported register bank for control of the on-board radio from a VME host.

- Digital Body Bug: Designed 2 FPGAs (Xilinx Virtex-E) and all the firmware and supporting applications for a Digital Body Bug System. This system comprised a tiny concealable transmitter/microphone module as well as a rack mountable receiver/listening unit. Audio was digitized to AES-EBU standards and then packetized into a proprietary format for RF transmission. Audio sampling rate and sample word size were user selectable. The transmitter FPGA controlled a Crystal Semiconductor AES-EBU encoding A/D as well as packetizing the audio data and applying Viterbi half-rate encoding. The receiver FPGA interfaced to a PC parallel port and controlled tuning of a frequency synthesizer chip as well as controlling the de-packetizing and AES-EBU decoding. A PC application was designed to allow the user to choose RF frequencies and audio sample parameters.

1998 – 2000 Consulted for Zeus Wireless of Columbia, Maryland. Projects as follow:

- Bluetooth RF Control Converter: Designed a Xilinx FPGA (Virtex-E) to convert control signals from an Ericsson Bluetooth Baseband Controller to a Zeus Wireless designed RF module. The FPGA performed realtime translation from Ericsson's JTAG-like control signals to Zeus' proprietary format. Successful Bluetooth connections were obtained using an Ericsson development board which was modified to hold the FPGA and the Zeus RF module while disabling the Ericsson RF circuitry.

- Palm CDPD Data Transmission Application: Developed a Palm handheld application which controlled a Sierra Wireless SB320 CDPD wireless modem. The application provided power-on initialization, dialtone recognition, call initiate and reception for the modem. It also implemented a Zeus proprietary packet transmission protocol called "NoError". This protocol was also implemented in a PC application program and successful tests were conducted with data passed from PC to Palm (and vice versa) across the public CDPD network with no data loss.

- Bit-Error-Rate Tester: Designed a Xilinx FPGA (Virtex) which utilized an m-sequence linear shift register to generate test data for transmit. After adjusting for channel delay, the received data was compared against the transmitted data and errors were accumulated. The FPGA could be interfaced to a PC parallel port for test control and error rate reporting.

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- 2.4 GHz Spread Spectrum Transceiver: Designed and coded all firmware for a frequency hopping transceiver. Initially this was implemented on a Siemens 8051 microprocessor variant. Later the code was ported to the Renesas M16C62. Handed off code when product was nearing commercial production. Then helped develop Store-and-Forward firmware to run on the same commercial hardware. This firmware ran under the CMS-RTX realtime operating system. Firmware was designed to be user upgradeable by reburning flash memory under control of a PC application.

1997 – 1998 Consulted for Gray Technologies of White Marsh, Maryland. Designed and coded embedded firmware for the LAMPS Avionic Radar project. All firmware executed on Analog Devices Sharc DSP chips under the SPOX realtime operating system. Developed a boot loading protocol which transferred 4 unique code images from a single huge flash memory module to 151 Sharc DSP chips populated across 18 boards upon system power-up. Also wrote a multiprocessing development, debugging, and diagnostic kernel to be used for further algorithm firmware development. Wrote driver to control UTMC Summit MIL-STD-1553 Avionics Bus interface. The system also supported loading of new radar processing firmware "on-the-fly" via the 1553 bus. Developed test procedures for all firmware.

1993 – 1996 Consulted for Zeus Technology Systems of Linthicum, Maryland. Designed and coded embedded firmware for a wide variety of commercial products: tunable wide-band satellite up-converter and down-converter, battery powered remote frequency sensor/counter, 6-channel SCPC satellite receiver, remote IF pan display, CD quality digital audio stereo microphone transmitter and receiver, QPSK satellite signal simulator, 2 GHz frequency hopping cordless phone. Performed primary system integration for all products. The SCPC satellite receiver and remote IF pan display both utilized an advanced graphics processor IC to provide a fast realtime graphical user interface and oscilloscope-like data display. Also designed Altera MAX7000, FLEX8000 and Xilinx 4000 FPGAs for several of the aforementioned products using both HDL and schematic entry. One FPGA design was migrated to a commercial ASIC at Rohm Semiconductor .

1993 – 1994 Consulted for Capitol Multimedia, Inc. of Bethesda, Maryland. Designed and coded a digital audio mixing system to generate music and sound effects for MSDOS and extended MSDOS PC games and multimedia titles. The system responded to multiple asynchronous realtime events mixing the desired sound effects into a single 16-bit stereo output. Also coded the CDROM game "NFL Football Trivia" which was released commercially in the fall of 1994. This was a large project which encompassed the playback of over 500 Mbytes of compressed motion and still video images in synchronization with multiple digital audio streams in response to user input.

1993 Consulted for Martin Marietta Research Laboratories of Baltimore, Maryland. Designed and coded realtime C language embedded firmware for the Arrow missile project. Completed a detailed software design specification prior to coding. Firmware modules included built in self test, process scheduling, and process execution. The firmware ran on a multiprocessor architecture of INMOS T805 Transputers and Analog Devices ADSP21000 DSPs. Performed system integration of firmware with several hardware subsystems.

1992 – 1993 Consulted for W.L. Gore & Associates of Newark, Delaware. Designed and coded a microwave connector and cable CAD program. The program provided complete design, simulation, and analysis functions for microwave and RF one and two-port systems. It ran under MSDOS and utilized the PharLap DOS extender to run in 80X86 protected mode. The program featured a user-friendly mouse, menu, dialog box interface that was designed and coded from scratch, but which closely resembled the MSWindows graphical user interface. The major program elements were the interactive graphical design and editing (side view & cross section) of connector and cable components, the modeling of complex frequency domain s-parameters from the component's mechanical dimensions, and a multitude of data analysis and graphing functions. Some of the analysis options included parameter conversions (g,h,y,z,abcd parameters, input impedance and admittance, etc.), graphing (magnitude, 20 log magnitude, real, imaginary, SWR, group delay, polar plot, smith chart, etc.), and time domain FFT conversion with optional windowing and step/impulse response. The project was taken from initial conception to the final release.

1991 – 1992 Consulted for M/A-COM GPI of Hunt Valley, Maryland. Designed all the firmware for the R/E-126 UHF/VHF scanning receiver controller. Responsibilities included code modules for bit mapped LCD display, graphics primitive generation, and user interface screens. Also designed modules for realtime interrupt management, multiple channel interrupt driven serial I/O and a wide variety of scanning receiver control functions. The firmware was written in C++ language with optimizations being done in 8086 assembly language. All modules were initially simulated on a PC under MSDOS and were then integrated into a STD-BUS 8088 embedded system. The project was taken from initial conception to the final production line.

1990 – 1991 Employed by Microprose Games of Hunt Valley, Maryland. Wrote C and 8051 assembly language firmware modules

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for the custom sound effects and music generating hardware subsystem of a coin-operated arcade game. The modules formed an operating system that provided music sequencing, realtime sound effect generation, and digitized speech playback. Wrote MSDOS hosted development tools (in C) for creating and editing sound effects. The sound effects were subsequently downloaded into custom hardware for use in arcade games. Supervised the PC board layout and routing of the sound effects and music generating hardware for an arcade game. This hardware was a complex mixture of digital and analog components that required extensive hand routing to insure optimal audio quality. Researched 3-D sound technology and DSP techniques for use in future arcade audio hardware systems. Completed preliminary design of a sound board utilizing a wavetable synthesis IC controlled by a 68000 microprocessor for digital sound reproduction.

1989 Consulted for CyberGraphics of Manchester, New Hampshire. Ported a large UNIX newspaper publishing application to run on Macintosh computers under the AUX operating system. Assisted on a port of the same application to Sun 4 workstations running the Sun OS.

1987 - 1989 Employed by Raytheon Missile System Division of Bedford and Tewksbury, Massachusetts. Wrote ADSP-2100 assembly language firmware modules for the digital signal processing subsystem of the Advanced Tactical Patriot missile program. The modules performed task scheduling, radar processing support and hardware self-test procedures. Designed digital and analog hardware I/O modules for the Advanced Tactical Patriot missile program. These modules interfaced to a multiprocessor (68020) 32-bit bus. The designs were taken through schematic capture, simulation, bread-board test/debug and form-factor artwork stages. Worked on a proposal for the digital signal processing subsystem of the Advanced Air-to-Air Missile. Tasks included evaluating signal processing algorithms and doing a feasibility study on the implementation of these algorithms in hardware via semi-custom ASICs.

1988 – 1989 Consulted for Interactive MicroSystems, Inc. of Haverhill, Massachusetts. Wrote commercial application software for the AMIGA family of microcomputers. The software allowed the interfacing of a microcomputer to any infrared remote controlled device such as a video tape recorder or CD player. Also wrote and self-marketed two commercial AMIGA software applications. One application featured realtime cooperation between independently executing processes for musical performances. A second application used digital signal processing techniques to modify sampled audio data.

1985 – 1986 Employed at The Pennsylvania State University by the Nuclear Engineering Department's Office of Energy and Technology Projects. Designed and constructed a variety of electronic audio-visual displays for educational programs. Taught introductory microprocessor theory and robotics to teacher-in-service groups. Managed the Reactor Sharing Program for the Breazeale Nuclear Reactor.

1983 – 1984 Worked on the NASA Space Shuttle Get Away Special Project sponsored by General Electric Corporation and Penn State's College of Engineering. Managed the electronics group responsible for payload power, experiment sequencing and data acquisition. Performed circuit design and construction utilizing both microprocessor-based (NSC-800) digital and transducer oriented analog elements.

Miscellaneous:

- Hobbies - music (listening & performance, wide-ranging eclectic tastes), hiking (A.T. section hiker), disc golfing, skiing (downhill & XC), biking, social dancing, reading
- References - available on request
- Availability - immediate